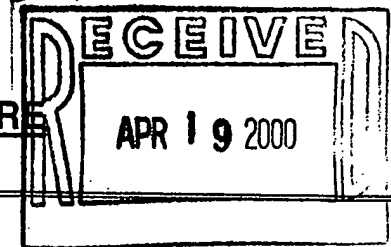




INVENTION DISCLOSURE



For Legal Department use only

Disclosure No.	<u>APD1692-HUS</u>	Cost Center No.	<u>4523</u>
Date Submitted:	<u>4-19-2000</u>	Division:	<u>DSP</u>
		Vice President:	<u>Bob Conrad</u>

(Where Necessary, Use Reverse Side or Separate Sheet to Complete Answers).

1. Title of the Invention: Turbo and Viterbi channel decoding implementation

[Note: The first-listed inventor will be considered the primary inventor and primary contact for patent matters.]

2. Full Name of Inventor No. 1. (including middle name or initial, "Jr.", etc.)
Stephen J. Plante

Full Name of Inventor No. 2. (including middle name or initial, "Jr.", etc.)
Zvi Greenfield

If more than three inventors, please use separate sheets.

The Invention

3. Brief description of problem solved by invention, and of the invention itself (big-picture overview of invention - may be illustrated by attaching block diagrams, flow charts, etc.):

Efficient implementation of the channel decoding algorithms known as Turbo Decoder and Viterbi Decoder. There are several aspects to the invention: parallel implementation of the algorithms (Trellis decoder) and hardware implementation on the ADSP-TS00x DSP. The algorithmic aspect is a SIMD style implementation of trellis decoders. For Turbo decoders, the SIMD style extends to the forward and reverse trellis flow.

4. Detailed description and sketches of invention are to be found on the attached sheets, identified below:

ADSP-TS001 Accelerator Architecture & Micro-Architecture Definition

ADSP-TS001 Forward Error Correction Acceleration Proposal

ADSP-TS001 Forward Error Correction Acceleration Proposal Presentation

ADSP-TS001 Channel Decoding "Soft" Acceleration on the TigerSHARC DSP

ADSP-TS001 Channel Decoding "Soft" Acceleration on the TigerSHARC DSP Presentation

5. List any formal drawings, schematics, manuals (by chapter and section), etc. which describe the invention and its operating environment.

Please see above listed documents

6. Into what product(s) will this invention go, or what product(s) will this invention be used to make, test, design, etc. (include future generations).

ADSP-TS00x Family of Digital Signal Processors

The Prior Art

7. Closest prior art practices known to the inventor(s), including products/activities of Analog.
None

8. List any tangible record of prior art/practices known to the inventor(s) e.g., products, patents, manufacturing processes, brochures, printed publications, seminar presentations, product demos, etc.

9. Brief description of the reasons that the invention is different from the prior art practices, and of the advantages resulting from those differences.

Invention Process and Documentation

10. The invention was first thought of on (date) 7/28/99, as evidenced by (notebook entry, etc.) Example program written to test concept.

11. The first written description of the invention occurred on (date) 12/17/99, a copy of which is attached.

12. The first drawing or sketch occurred on (date) 1/24/00, a copy of which is attached.

13. The first disclosure of the invention to others within Analog, occurred on (date) 12/20/99, as evidenced by Power point presentation for internal discussion of proposed solution

14. The invention was first shown to be operable in its intended environment on (date) 7/28/99
by: Stephen Plante
(computer simulation, working prototype, process implementation, etc.) as evidenced
by: Computer Simulation

[Answer questions 15 and 16 if applicable. If inapplicable, write "N/A" in the appropriate blanks.]

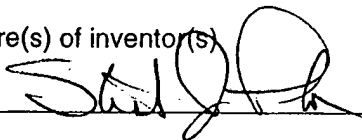
15. The first disclosure of the invention to anyone outside of Analog (if any) occurred on (date) 2/8/2000 to Siemens in Munich.

(pursuant to/not pursuant to a confidentiality [NDA] agreement, dated on file , copy attached).

16. The invention was first sold, sampled, offered for sale, or used to produce a product that ultimately was sold, on (date) N/A as evidenced by: N/A

17. Signature(s) of inventor(s)

(1)



Date

4/7/00

(2)

Date

(3)

Date

18. Signature(s) of witness(es)

(1)

Date

(2)

Date

(3)

Date

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